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10/034,458	12/28/2001	Gyo Un Choi	CU-2797 VE	9340

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/034,458	Applicant(s) CHOI ET AL.	
	Examiner José R Díaz	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show, for example, the structure described on page 9, lines 1-10 and 16-21 of the specification, in which the reference number 17a is the data odd pad connected to the date odd line (D_1, D_3 ... D_{2+n}) and the reference number 17b is the data even pad connected to the data even line (D_2, D_4 ... D_{2+n}). Further, Figures 2 and 3A fails to shows the pixels described on page 2, line 13. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "17b" has been used to designate both "data even pad" and "data even line", and the reference character "17a" has been used to designate both "data odd pad" and "data odd line" (see page 9, lines 8-10). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid

abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. A substitute specification including the claims is required pursuant to 37 CFR 1.125(a) because the specification appears to be a literal translation into English from a foreign document and replete of confusing and circular statements. For instance, applicant, as stated before, describes a structure in which the data odd pad and data even pad are 17a and 17b, respectively. However, figures 3B, 4A and 4B disclose that the data odd pad is 17b instead of 17a, and the data event pad is 17a instead of 17b. Moreover, the specification describes a testing structure for detecting defects of what it seems to be a partial LCD structure (page 5, lines 13-20). However, figures 4a and 4b shows a structure in which the defect detected are not from the partial LCD structure but from the testing structure per se. A substitute specification filed under 37 CFR 1.125(a) must only contain subject matter from the original specification and any previously entered amendment under 37 CFR 1.121. If the substitute specification contains additional subject matter not of record, the substitute specification must be filed under 37 CFR 1.125(b) and (c).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 9-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The structure recited in claims 9-12 requires the formation of pixels in the TFT array. However, figures 3A-4B contradict the recited limitation by showing a TFT array (11) in which the pixels are missing. Does figure 3A shows a partial LCD structure, a LCD structure in which the pixels are not shown, or a test structure that is connected to a LCD structure (not shown in the figure 3A)?

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3, 5-7, 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by applicant's admitted prior art.

Regarding claims 1, applicant acknowledges a structure comprising: a TFT array unit (11) comprising a plurality of gate lines ($G_1 \ldots G_n$) and data lines ($D_1 \ldots D_n$) formed in

a matrix shape (see figure 2), having TFT transistors at the intersection of the gate line and the data line (see figure 2 and page 2, line 13); a data pad unit (17a, 17b) commonly connected to the plurality of data lines ($D_1 \ldots D_n$), receiving signals from driving the data lines (see fig. 2); and a wiring unit (consider the cone shaped wiring units extended between the pixel array (11) and the data pads (17a, 17b)) for testing defects of data line, connected between the data pad unit and the data line, testing disconnection and short of the data line (see fig 2 and page 2, lines 16-20).

Regarding claim 2, applicant acknowledges a structure comprising a first data pad unit (17a) commonly connected between odd data lines of the plurality of data lines, and a second data pad unit (17b) commonly connected between even data lines of the plurality data lines (see fig. 2).

Regarding claim 3, applicant acknowledges a structure comprising a first wiring unit (consider the wiring portions of the cone shaped wiring units extended between the pixel array (11) and the data pad (17a), and connected to the odd lines $D_1 \ldots D_{n+2}$) for testing defects of data line connected between the first data pad unit (17a) and the odd data line (D_1), and a second wiring unit (consider the wiring portions of the cone shaped wiring units extended between the pixel array (11) and the data pad (17b), and connected to the even lines $D_2 \ldots D_{n+2}$) for testing defects of data line connected between the second data pad unit (17b) and the even data line (D_2) (see fig. 2).

Regarding claim 5, applicant acknowledges a structure comprising: a TFT array unit (11) comprising a plurality of gate lines ($G_1 \ldots G_n$) and data lines ($D_1 \ldots D_n$) formed in a matrix shape (see figure 2), having TFT transistors at the intersection of the gate line

and the data line (see figure 2 and page 2, line 13); a gate pad unit (15a, 15b) commonly connected to the plurality of gate lines ($G_1 \ldots G_n$), receiving signals from driving the gate lines (see fig. 2); and a wiring unit (consider the cone shaped wiring units extended between the pixel array (11) and the gate pads (15a, 15b)) for testing defects of gate line, connected between the gate pad unit and the gate line, testing disconnection and short of the gate line (see fig 2 and page 2, lines 16-20).

Regarding claim 6, applicant acknowledges a structure comprising a first gate pad unit (15a) commonly connected between odd data lines of the plurality of data lines, and a second gate pad unit (15b) commonly connected between even data lines of the plurality data lines (see fig. 2).

Regarding claim 7, applicant acknowledges a structure comprising a first wiring unit (consider the wiring portions of the cone shaped wiring units extended between the pixel array (11) and the gate pad (15a), and connected to the odd lines $G_1 \ldots G_{n+2}$) for testing defects of gate line connected between the first gate pad unit (15a) and the odd gate line (G_1), and a second wiring unit (consider the wiring portions of the cone shaped wiring units extended between the pixel array (11) and the gate pad (15b), and connected to the even lines $G_2 \ldots G_{n+2}$) for testing defects of gate line connected between the second gate pad unit (15b) and the even data line (G_2) (see fig. 2).

Regarding claims 9-11, applicant acknowledges a structure comprising: a TFT array unit (11) comprising a plurality of gate lines ($G_1 \ldots G_n$) and data lines ($D_1 \ldots D_n$) formed in a matrix shape (see figure 2), having TFT transistors at the intersection of the gate line and the data line (see figure 2 and page 2, line 13); a common voltage pad unit

(13) commonly connected to the common voltage line connected to each pixel (see page 2, lines 12-14); and a wiring unit (consider the portion of the common voltage line close to the common voltage pad unit (13) as the wiring unit) connected between the common voltage line and the common voltage pad unit, testing disconnection and short of the common voltage line (see fig 2 and page 2, lines 12-20).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. As far as understood, claims 4, 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Chung et al. (US Pat. No. 6,356,320 B1).

Regarding claims 4, applicant's admitted prior art fails to teach a wiring unit having a zigzag shape. Chung et al. teaches that it is well known in the art to form a zigzag-wiring unit (85, G1, G2, G3, G4) (see Figs. 7-8, abstract and col. 4, lines 34-49). Applicant's admitted prior art and Chung et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a zigzag-wiring unit. The motivation for doing so, as is taught by Chung et al., is eliminating stitching defects (abstract and col. 6, lines 10-17). Therefore, it would have been obvious to combine Chung et al. with Applicant's admitted prior art to obtain the invention of claims 4, 8 and 12.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shimizu (US Pat. No. 5,652,632) discloses a LCD apparatus comprising pixels ($E_{11}...E_n$) in a TFT array ($Q_{11}...Q_n$) (see Fig. 2) having a zigzag resistance (8(L)) connected to the pad units (P_{xn}, P_{yn}) (see Fig. 7A). Hioki et al. (US Pat. No. 6,088,073) discloses the formation of a zigzag structure (41) (see Fig. 5A). And Okumura (US Pat. No. 4,884,875) discloses liquid crystal device comprising a zigzag structure (11) connected to the voltage electrode (16) (see fig. 4).

Correspondence

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GEORGE ECKERT
PRIMARY EXAMINER

JRD